Docket No. 5000-5291

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Takefumi NISHIMUTA; Hiroshi MIYAGI; Tadahiro OHMI; Shigetoshi SUGAWA; and Akinobu TERAMOTO		
Serial No.:	TBA	Group Art Unit:	TBA
Filed:	Herewith	Examiner:	TBA
For:	MIS TRANSISTOR AND CMOS TRANSISTOR		
Customer No.:	27123		

INFORMATION DISCLOSURE STATEMENT

Mail Stop
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to Rule 56, applicant hereby calls the attention of the Patent Office to the references listed on the attached Form PTO 1449. Copy(ies) of these references ☒ are attached ☐ were filed in related application U.S. Serial No(s) _____, filed _____, respectively.

☐ This document is being filed within three (3) months of the filing date of the application

☐ Please charge the $180 fee to Deposit Account No. 13-4500, Order No. _____.

☒ This document is being concurrently filed with the above-identified application

☐ This document is being concurrently filed with an Request for Continued Examination (RCE)

☐ This document is being filed prior to a first Office Action

☒ This document is accompanied by a Search Report/Communication cited in a corresponding PCT or foreign counterpart application.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required for this Information Disclosure Statement, or credit any overpayment to Deposit Account No. 13-4500, Order No. 5000-5291. A DUPLICATE COPY OF THIS SHEET IS ATTACHED.

Respectfully submitted,
MORGAN & FINNEGAN, L.L.P.

Dated: December 13, 2005

By: Steven F. Meyer
Steven F. Meyer
Registration No. 35,613

Correspondence Address:

Morgan & Finnegan, L.L.P.
3 World Financial Center
New York, New York 10281-2101
(212) 415-8700 Telephone
(212) 415-8701 Facsimile

962125 v1

FORM PTO-1449 INFORMATION DISCLOSURE CITATION	Attorney Docket No. 5000-5291	Serial No.: To Be Assigned
	Applicants: Takefumi NISHIMUTA; Hiroshi MIYAGI; Tadahiro OHMI; Shigetoshi SUGAWA; and Akinobu TERAMOTO	
	Filing Date: Herewith	Group Art Unit: To Be Assigned

U.S. PATENT DOCUMENTS

Examiner Initial		Patent Number	Publication Date	Name	Class	Sub-Class	Filing Date
		2002/0185676	December 12, 2002	Momose	257	327	July 30, 2001
		2004/0102052	May 27, 2004	Ohmi et al	438	765	December 27, 2001

FOREIGN PATENT DOCUMENTS

Examiner Initial		Patent Number	Publication Date	Country	Class	Sub-Class	Translation
		2002-110963	April 12, 2002	JAPAN	H 01 L	29 / 78	Accompanied by English abstract
		2002-359293	December 13, 2002	JAPAN	H 01 L	21 / 8238	Accompanied by US Publication No. 2002/0185676
		8-264764	October 11, 1996	JAPAN	H 01 L	29 / 78	Accompanied by English abstract
		7-249768	September 26, 1995	JAPAN	H 01 L	29 / 78	Accompanied by English abstract
		2002-261091	September 13, 2002	JAPAN	H 01 L	21 / 316	Accompanied by US Publication No. 2004/0102052
		9-023011	January 21, 1997	JAPAN	H 01 L	29 / 786	Accompanied by English abstract
		63-228662	September 22, 1088	JAPAN	H 01 L	27 / 08	Accompanied by English abstract
		1-276669	November 7, 1989	JAPAN	H 01 L	29 / 78	Accompanied by English abstract

OTHER DOCUMENTS (Including Author, Title, Date, etc.)

		Partial English translation of office action for corresponding Taiwanese Patent Application and Taiwanese Office Action.
		Hisamoto et al, "FinFET – A Self-Aligned Double-Gate MOSFET Scalable to 20nm", *IEEE Transactions on Electron Devices*, Vol 47, No. 12, pps 2320-2325, December 12, 2000
		Y. Choi et al, "FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering", *Electron Devices Meeting, IEDM 02 Digest*, pps 259-262, December 2002
		Y. Choi et al, "Nanoscale CMOS Spacer FinFET for the Terabit Era", *IEEE Electron Device Letters*, Vol 23, No. 1, pps 25-27, January 2002

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered Include copy of this form with next communication to Applicant.

962161 v1